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APPLICATION FOR UNITED STATES LETTERS PATENT

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FOR: **TEST CIRCUIT FOR LOGICAL INTEGRATED CIRCUIT AND METHOD FOR TESTING SAME**

DOCKET NO.: **PNDF-01197**

TEST CIRCUIT FOR LOGICAL INEGRATED CIRCUIT AND MTHOD FOR TESTING SAME

BACKGROUND OF THE INVENTION

The invention relates to a test circuit for a logical integrated circuit and a method for testing the same which measure an alternating current (AC, hereinafter) characteristic of a logical integrated circuit by using a scan path technique in which plural flop-flops (FFs, hereinafter) of the scanning type are successively connected in series and a test pattern is propagated therealong, and especially to a test circuit for a logical integrated circuit and a method for testing the same in which time spent in measuring an AC characteristic of each of input and output terminals of a logical integrated circuit can be shortened.

FIELD OF THE INVENTION

A scan path technique is one of DFT (design for test) techniques for simplifying a procedure for generating a test pattern of a logical integrated circuit which is increasing its scale steadily, and makes it possible to control or to observe a state of a desired FF by relacing the FFs in the logical integrated with the FFs of the scanning type. Since a sequence circuit can be treated as a combinational circuit by using the scan path technique, the test pattern which has been written out by manual works hitherto can be written out automatically by using an Automatic Test Pattern Generator (ATPG, hereinafter) in combination with the scan path technique, and a period of time necessary for writing out the test pattern can be sharply reduced.

According to the ATPG, it becomes possible to write out the test pattern which is applied only to a desired portion on the logical integrated circuit, such as an interval between given FFs for instance, so that the data are distributed thereon in a desired state. By utilizing the aforementioned feature, the test pattern to be applied to a path between an external terminal and a desired FF is written out, and the AC characteristics, such as a transition time, a set up time, a hold time, etc. of a waveform of an output signal of the logical integrated circuit are measured on a Large Scale Integrated circuit (LSI, hereinafter) tester.

With the development of the scan path technique, it becomes possible to generate the test pattern for measuring AC characteristics of the input and output terminals of the logical integrated circuit. Accordingly, the number of the test patterns can be decreased as compared with the conventional method for inspecting the AC characteristics of the logical integrated circuit, and the test time is shortened. However, in the present situation, shortening of the test time is further requested in order to decrease the cost of the device.

In case that the test pattern is generated by using the scan path technique, a greater part of the test time is spent in a state that the signal is successively shifted on the scan path forming a shift register. This situation is caused by the fact that the data captured in an ordinary mode is successively shifted on the scan path in the scan shift mode till the data arrives at the external terminal. Since the scan path becomes long in the large scale integrated circuit, time spent in the scan shift mode becomes long, and the number of the test patterns and the test time increase

as a result.

For example, the test circuit 400 shown in FIG.1 is composed of m×n FFs arranged in the form of a matrix, in which the m FFs composed of the FF411, the FF421 to the FF4m1 form the first (front) stage located the closest to the input terminals of the test circuit, those composed of the FF412, the FF422 to the FF42m form the second stage of the same, and so on. Finally, the m FFs composed of the FF41n, the FF42n to the FF4mn form the n th (final) stage located the closest to the output terminals of the test circuit. As mentioned in the above, the test circuit is composed of the n stages, each of which is composed of the m FFs.

In the scan path in the convention test circuit 400 shown in FIG.1, a scan input SIN is connected with an input terminal of the FF411 standing at the head of the first stage. Thereafter, the FF411, the FF421 to the FF4m1 are successively connected in series in the first stage. Then, an output terminal Q of the FF4m1 standing at the end of the first stage is connected with an input terminal of the FF412 standing at the head of the second stage, and the FF412, the FF422 to the FF42m are successively connected in series in the second stage. After similar processes are repeated in the respective stages, all the FFs arranged in the first to n th stages are successively connected in series, and, finally, an output terminal Q of the FF4mn standing at the end of the n th stage is connected with a scan output SOT.

Next, a procedure for generating a test pattern which measures the AC characteristic of the input terminal of the test circuit shown FIG.1 will be considered. Since the signal taken in a FF is successively shifted to the following FF on the scan

path till the signal propagates to the scan output SOT, in case that there are 50,000 (=m×n) FFs on the scan path and the test signal supplied from the input terminal IN1 is taken in the FF411 standing at the head of the first stage of the test circuit, it becomes necessary to repeat the scan shifts 50,000 times till the signal supplied from the input terminal IN1 propagates to the scan output SOT.

On the other hand, in case that the test pattern for measuring the AC characteristics of the output terminals OT1 to OTm is generated, since the signal is transmitted to the scan output SOT, it becomes necessary to repeat the scan shifts 50,000 times, because there are 50,000 FFs on the scan path which extends to the FF4mn standing at the end of the n th stage of the test circuit.

In general, the FFs on the scan path are connected in the order of the instance name of the FF by using a scan path-inserting tool as shown in FIG.1. As a result, there arise incommodities that the many scan shifts become necessary in some cases as mentioned in the above, and increases of the number of the test patterns and time spent in the test are brought upon.

With an object of resolving the point at issuer that time spent in generating the test patterns or in performing a board test increases in the large scale integrated circuit, an integrated circuit and a method for testing the same are disclosed in Japanese Patent, No.309204.

In the aforementioned test circuit 500 shown in FIG.2, a scan input SIN is connected with an input terminal of a FF511 standing at the head of the first stage of the test circuit, and the FF511 to the FF5m1 are connected in series similarly to the test circuit

shown FIG.1. However, an output terminal of the FF5m1 is connected with an input terminal of the FF51n standing at the head of the n th stage of the test circuit, and, thereafter, the FF51n to the FF5mn are connected in series. An output terminal of the FF5mn standing at the end of the n th stage is connected with a right terminal of a selector 501.

The output terminal of the FF5mn standing at the end of the n th stage of the test circuit is connected with an input terminal of the FF512 standing at the head of the second stage of the test circuit. The FFs arranged in the second to (n-1) th stages (the internal FFs, hereinafter) are successively connected in series, the end of which is connected with the left input terminal of the selector 501. The selector 501 selects either a scan path formed only of the FFs located the closest to the input and output terminals or the other scan path formed of all the FFs arranged in the integrated circuit, and connects the end of the selected scan path with the scan output SOT. Accordingly, time spent in measuring the AC characteristic of each of the input and output terminals is determined depending only on the number of the scan shifts on the scan path which is formed only of the FFs located the closest to the input and output terminals.

However, there is yet room for improvement in the conventional test circuit for the logical integrated circuit shown in FIG.2, and whether the test time can be further decreased or not is open to discussion.

That is to say, in case that a test pattern is inputted from the input terminal INx, it is necessary to scan all the FFs on the scan path which ranges from the input terminal INx to the m

FFs located the closest to the output terminals in order to output the data from the scan output SOT.

SUMMRY OF THE INVENITON

Accordingly, it is an object of the invention to settle the aforementioned problems, and to provide a test circuit for a logical integrated circuit and a method for testing the same in which time spent in measuring AC characteristics of input and output terminals of a logical integrated circuit can be further reduced.

According to the first feature of the invention, a test circuit for a logical integrated circuit comprises:

plural flip-flops of a scanning type (FFs, hereinafter) arranged in the first to n th stages, in each of which the FFs are successively connected in series,

plural logic gates, output terminals of which are respectively connected with input terminals of the plural FFs, and

a scan path which is formed of a series connection of a part or the whole of the plural FFs, and propagates a test pattern for measuring an AC characteristic of an input or output terminal of the logical integrated circuit,

wherein the scan path connects an output terminal of the FF standing at the end of the first stage with a scan output.

According to the second feature of the invention, a test circuit for a logical integrated circuit comprises:

plural FFs arranged in the first to n th stages, in each of which the FFs are successively connected in series,

plural logic gates, output terminals of which are respectively connected with input terminals of the plural FFs, and

a scan path which is formed of a series connection of a part or the whole of the plural FFs, and propagates a test pattern for measuring an AC characteristic of an input or output terminal of the logical integrated circuit,

wherein the scan path connects a scan input with an input terminal of the FF standing at the head of the n th stage.

According to the third feature of the invention, a test circuit for a logical integrated circuit, comprises,

plural FFs arranged in the first to n th stages, in each of which the FFs are successively connected in series,

plural logic gates, output terminals of which are respectively connected with input terminals of the plural FFs, and

a scan path which is formed of a series connection of a part or the whole of the plural FFs, and propagates a test pattern for measuring an AC characteristic of an input or output terminal of the logical integrated circuits,

wherein the scan path connects a scan input with an input terminal of the FF standing at the head of the n th stage,

again successively connects the FFs arranged in the second to (n-1) th stages in series, after restarting from an output terminal of the FF standing at the end of the n th stage,

once again connects an output terminal of the FF standing at the end of the (n-1) th stage with an input terminal of the FF standing at the head of the first stage, and

finally connects an output terminal of the FF standing at the end of the first stage with a scan output.

According to the aforementioned structures, a test pattern inputted to an input terminal of the test circuit is transmitted to the scan output, after the scan shifts are repeated only in the FFs arranged in the first stage. On the other hand, a test pattern inputted to the scan input is transmitted to each of the output terminals of the test circuit, after the scan shifts are repeated only in the FFs arranged in the n th stage.

According to the fourth feature of the invention, a method for testing a logical integrated circuit, which is compose of:

plural FFs arranged in the first to n th stages, in each of which the FFs are successively connected in series,

plural logic gates, output terminals of which are respectively connected with input terminals of the plural FFs, and

a scan path which is formed of a series connection of a part or the whole of the plural FFs, and propagates a test pattern for measuring an AC characteristic of an input or output terminal of the logical integrated circuit, comprises the steps of:

connecting an output terminal of the FF standing at the end of the first stage with a scan output,

inputting a clock signal to a clock signal input terminal,

inputting a predetermined data signal to one of the input terminals of the logical integrated circuit, and

measuring the AC characteristic of the one of the input terminals of the logical integrated circuit by inspecting an output of the scan output.

According to the fifth feature of the invention, a method for testing a logical integrated circuit, which is composed of:

plural FFs arranged in the first to n th stages, in each of which the FFs are successively connected in series,

plural logic gates, output terminals of which are respectively connected with input terminals of the plural FFs, and

a scan path which is formed of a series connection of a part or the whole of the plural FFs, and propagates a test pattern for measuring an AC characteristic of an input or output terminal of the logical integrated circuit, comprises the steps of:

connecting a scan input with an input terminal of the FF standing at the head of the n th stage,

inputting a clock signal to a clock signal input terminal,

inputting a predetermined data signal to a scan input, and

measuring an AC characteristic of one of the output terminals of the logical integrated circuit by inspecting an output of the one of the output terminals.

According to the sixth feature of the invention, a method for testing a logical integrated circuit, which is composed of:

plural FFs arranged in the first to n th stages, in each of which the FFs are successively connected in series,

plural logic gates, output terminals of which are respectively connected with input terminals of the plural FFs, and

a scan path which is formed of a series connection of a part or the whole of the plural FFs, and propagates a test pattern for measuring an AC characteristic of an input or output terminal of

the logical integrated circuit, comprises the steps of:

connecting a scan input with an input terminal of the FF standing the head of the n th stage,

connecting the FFs arranged in the second to (n-1) th stages successively in series, after restarting from an output terminal of the FF standing at the end of the n th stage,

connecting an output terminal of the FF standing at the end of the (n-1) th stage with an input terminal of the FF standing at the head of the first stage,

connecting an output terminal of the FF standing at the end of the first stage with a scan output,

inputting a clock signal to a clock signal input terminal,

inputting a predetermined data signal to one of the input terminals of the logical integrated circuit, and

measuring the AC characteristic of the one of the input terminals of the logical integrated circuit by inspecting an output of the scan output.

According to the seventh feature of the invention, a method for testing a logical integrated circuit, which is composed of:

plural FFs arranged in the first to n th stages, in each of which the FFs are successively connected in series,

plural logic gates, output terminals of which are respectively connected with input terminals of the plural FFs, and

a scan path which is formed of a series connection of a part or the whole of the plural FFs, and propagates a test pattern for measuring an AC characteristic of an input or output terminal of the logical integrated circuit, comprises the steps of:

connecting a scan input with an input terminal of the FF standing the head of the n th stage,

connecting the FFs arranged in the second to (n-1) th stages successively in series, after restarting from an output terminal of the FF standing at the end of the n th stage,

connecting an output terminal of the FF standing at the end of the (n-1) th stage with an input terminal of the FF standing at the head of the first stage,

connecting an output terminal of the FF standing at the end of the first stage with a scan output,

inputting a clock signal to a clock signal input terminal,

inputting a predetermined data signal to a scan input, and

measuring an AC characteristic of one of the output terminals of the logical integrated circuit by inspecting an output of the one of the output terminals.

BRIEF DESCRIPTION OF DRAWINGS

The invention will be explained in more detail in conjunction with appended drawings, wherein:

FIG.1 is a block diagram for showing a typical example of a conventional test circuit for a logical integrated circuit,

FIG.2 is a block diagram for showing the other example of a conventional test circuit for a logical integrated circuit,

FIG.3 is a block diagram for showing a test circuit for a logical integrated circuit according to the first preferred embodiment of the invention,

FIG.4 is a block diagram for showing a test circuit for a logical integrated circuit according to the second preferred

embodiment of the invention, and

FIG.5 is a block diagram for showing a test circuit for a logical integrated circuit according to the third preferred embodiment of the invention.

DESCRIPTION OF PREFERRED EMBODIMENTS

Next, preferred embodiments of the invention will be explained preferring to the appended drawings.

FIG.3 is a block diagram for showing the first preferred embodiment of the invention. A test circuit 100 for a logical integrated circuit is provided with input terminals IN1, IN2 to INi, INj, a clock signal input terminal CLK, output terminals OT1, OT2 to Otm, a scan input SIN, a scan output SOT, ad a scan enable terminal SE. As shown in FIG.3, the m×n FFs are arranged in the form of a matrix in the test circuit 100, that is to say, the n stages of the FFs, each of which is composed of the m FFs, are successively arranged to form the matrix formed of m rows and n columns. Explaining concretely, the m FFs composed the FF111, the FF121 to the FF1m1 form the first stage located the closest to the input terminals SIN to Inj, and the other m FFs composed of the FF11n, the FF12n to the FF1mn form the n-th (final) stage located the closest to the output terminals OT1 to OTm.

A higher input terminal of each FF of the scanning type is connected with the scan path, and a lower input terminal of the same is connected with an output terminal of a logic gate. Either the scan path or the logic gate is selected in accordance with a control voltage outputted from the scan enable terminal SE, and the data selected in this way is taken in the FF. An output terminal

Q of the FF is connected with a lower input terminal of the other FF located in the next stage via a logic gate on the one side, and with a higher input terminal of the following FF in the link forming the scan path on the other side.

The data signals inputted to the input terminals IN1, IN2 are supplied to the input terminals of the logic gate, the output of which is taken in the FF111 standing at the head of the first stage. The data signals inputted to the input terminals IN2, IN3 are supplied to the input terminals of the logic gate, the output of which is taken in the FF121. The data signals inputted to the input terminals INi, INj are supplied to the input terminals of the logic gate, the output of which is taken in the FF1m1. The FF11n located the closest to the output terminals supplies the output signal to the output terminal OT1. The FF12n supplies the output signal to the output terminal OT2. The FF1mn supplies the output signal to the output terminal OTm.

In a part of the scan path lying in the x th stage of the test circuit, the m FFs composed of the FF11x, the FF12x to the FF1mx are successively connected in series.

In the scan path of the test circuit 100 shown in FIG.3, the scan input SIN is connected with the input terminal of the FF11n standing at the head of the n th stage, and the m FFs composed of the FF11n to the FF1mn are successively connected in series. Then, the output terminal Q of the FF1mn standing at the end of the n th stage is connected with the input terminal of the FF112 standing at the head of the second stage. Thereafter, the internal FFs (the FFs arranged in the second to (n-1) th stages) are successively connected in series, and the FF1m (n-1) (not shown)

standing at the end of the (n-1) th stage is connected with the m FFs arranged in the first stage in series. Finally, the output terminal Q of the FF1m1 standing at the end of the first stage is connected with the scan output SOT.

Next, the operation of the test circuit 100 shown in FIG.3 will be explained referring to the appended drawings.

First, a procedure for generating a test pattern for measuring the AC characteristic of the input terminal IN1 will be discussed in case that the data applied to the input terminal IN1 changes into "1" from "0" and the data applied to the other input terminal IN2 is kept to be "1". When the data applied to the input terminals IN1, IN2 are respectively "0.1", a data "0" is taken in the FF111. When the data applied to the input terminals IN1, IN2 are respectively "1,1", the data "1" is taken in the FF111.

Accordingly, when the data "0.1" are respectively inputted to the input terminals IN1, IN2 in the first place, the data "0" is taken in the FF111. In the test circuit 100, since the m FFs composed of the FF111 to the FF1m1 are arranged in the final stage of the scan path and connected in series to form a shift register, the data "0" taken in the FF111 is successively shifted along the following FFs composed of the FF121 to the FF1m1, and finally transmitted to the scan output SOT, through which the data "0" can be observed.

Next, when the data "1,1" are respectively inputted to the input terminals IN1, IN2, the data "1" is taken in the FF111. Similarly to the above explanation, the data "1" can be observed through the scan output SOT.

By using the test pattern generated in this way, the time

when the data applied to the input terminal IN1 changes into "1" from "0" is shifted forward and backward, and whether the data inputted to the input terminal IN1 is taken in the FFs correctly or not is judged on the LSI tester. The AC characteristic of the input terminal IN1 can be seized from the delay time of the data signal relative to the clock signal on the basis of the aforementioned judgement.

On the other hand, in order to generate a test pattern for measuring the AC characteristic of the output terminal OTm in case that the data applied to the output terminal OTm changes into "1" from "0", it is necessary that the data applied to the output terminal Q of the FF1mn changes into "1" form "0". Accordingly, the data "0" is inputted through the scan input SIN in the first place, and the data "0" is taken in the FF11n.

Next, the data "1" is inputted through the scan input SIN, taken in the FF11n, successively shifted along the scan path, and observed through the output terminal OTm. The AC characteristics of the output terminal OTm can be seized by using the test pattern generated in this way.

In the above explanation, the test circuit is composed of the m×n FFs arranged in the form of a matrix, the first to n th columns of which respectively correspond to the first to n th stages of the test circuit. Each stage of the test circuit is composed of the m FFs connected in series, and the FFs arranged in the respective stages are connected in series in acordance with a predetermined order to form a scan path. However, the form of the arrangement of the FFs is never restricted to that of the matrix, an there is no limitation on the number of the FFs in each stage.

Moreover, although it is necessary to arrange the FFs connected in series the closest to both the input and output terminals, there is no limitation on the other FFs which are connected in series in the internal part of the test circuit, because these internal FFs are provided for the test circuit in accordance with the strictures and the combinations of the logic gates, and the arrangement of them is never restricted by the above explanations.

Next, the second preferred embodiment of the invention will be explained reffrring to FIG.4.

Since the arrangement of the input terminals INx, the output terminals OTx and the FF2mn in the test circuit 200 shown in FIG.4 is the same as that of the test circuit 100 shown in FIG.3, a detailed explanation thereon will be omitted. The distinction between the test circuits 100, 200 consists in the route of the scan path.

In the scan path of the test circuit shown in FIG.4, the scan input SIN is connected with the input terminal of the FF212 standing at the head of the second stage of the test circuit, and the output terminal Q of the FF2mn standing at the end of the n th stage is connected with the input terminal of the FF211 standing at the head of the first stage. Accordingly, a point of difference between the test circuit 200 shown in FIG.4 and the same 400 shown in FIG.1 consists in the fact the m FFs arranged in the first stage are connected with the scan output SOT in the test circuit 200 to form the scan path.

Similarly to the test circuit 100 shown in FIG.3, in case that a test pattern for measuring the AC characteristic of the input terminal IN1 in the test circuit 200 is generated, the data

signals are respectively inputted to the input terminals IN1, IN2, and the clock signal is inputted to the clock signal input terminal CLK. The data signals inputted to the input terminals IN1, IN2 are supplied to the input terminals of the logic gate, the output signal of which is taken in the FF211. The data taken in the FF211 is successively shifted along the scan path which connects the FF211 to the FF2m1 in series, transmitted to the scan output SOT, and observed therethrough.

By using the test pattern generated in this way, the time when the data signal is inputted through the input terminal IN1 is shifted forward and backward, and whether the inputted data signal is taken in the FFs correctly or not is judged. The AC characteristic of the input terminal IN1 is seized through the delay time of the data signal relative to the clock signal on the basis of the aforementioned judgement.

Next, the third preferred embodiment of the invention will be explained referring to FIG.5.

In the test circuit 300 shown in FIG.5, since the arrangement of the input and output terminals INx, OTx, and a FF3mn is the same as that shown in FIG.3, detailed explanations thereon will be omitted. The distinction between the test circuits 100, 300 consists in the route of the scan path.

That is to say, in the scan path of the test circuit 300 shown in FIG.5, the scan output SOT is connected with the output terminal Q of the FF3m(n-1) (not shown) standing at the end of the (n-1) th stage of the test circuit, and the output terminal Q of the FF3m1 standing at the end of the first stage is connected with the input terminal of the FF312 standing at the head of the second

stage. The distinction between the test circuit 400 shown in FIG.1 and the same 300 shown in FIG.5 consists in the fact that the m FFs arranged in the n th stage in the test circuit 300 is connected with the scan input SIN to form the scan path.

Similarly to the test circuit 100 shown in FIG.3, in order to generate the test pattern for measuring the AC characteristic of the output terminal OTm when the data applied thereto changes, since it is necessary that the data outputted from the FF3mn changes, the data is inputted through the scan input SIN, and taken in the FF31n in the first place. Since the FF31n to the FF3mn are connected in series to form the scan path in the test circuit 300, the data inputted through the scan input SIN is successively shifted along the FF32n to the FF3mn forming a shift register, and finally transmitted to the FF3mn. The data applied to the output terminal Q of the FF3mn can be observed through the output terminal OTm.

Next, the other data is inputted from the scan input SIN, and the data supplied to the input terminal of the FF31n can be observed through the output terminal OTm. The AC characteristic of the output terminal OTm can be seized by using the test patterns obtained by the aforementioned procedures.

As mentioned in the above, according to the invention, the AC characteristics of the input and output terminals can be respectively measured in a short time.

In the test circuit according to the invention, since each input terminal is connected with the scan output via the scan path which is formed only of the FFs arranged the closest to the input terminals, and, moreover, each output terminal is connected with the scan input via the scan path which is formed only of the FFs

arranged the closest to the output terminals, the number of the scan shifts in the test circuit according to the invention can be reduced by half approximately as compared with that in the conventional test circuit disclosed in Japanese Patent No. 309204, in which the scan path is formed of a series connection of the first plural FFs arranged the closest to the input terminals and the second FFs arranged the closest to the output terminals.

Although the invention has been described with respect to specific embodiment for complete and clear disclosure, the appended claims are not to be thus limited but are to be construed as embodying all modification and alternative constructions that may be occurred to one skilled in the art which fairly fall within the basic teaching herein set forth.